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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,435	10/28/2003	Gururaj Pangal	112-0123US	4461

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WONG, CABELLO, LUTSCH, RUTHERFORD & BRUCCULERI, P.C.
20333 SH 249
SUITE 600
HOUSTON, TX 77070

EXAMINER	
SUN, SCOTT C	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,435	PANGAL ET AL.	
	Examiner	Art Unit	
	Scott Sun	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/31/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/31/05 have been fully considered but they are not persuasive.

2. Examiner summarizes applicant's arguments as:

   a. Regarding claim 1, Yamamoto does not teach a switch, a control module, or data virtualization.

   b. Regarding claim 2 and 5, Yamamoto does not teach virtual target task or virtual initiator task.

   c. Regarding claim 3, Yamamoto does not teach virtual target or virtual initiator.

   d. Regarding claim 7 and 8, Examiner's reference does not correspond to port processors.

   e. Regarding claims 9 and 17 do not disclose a switch coupling host and storage.

3. Examiner's response to applicant's arguments:

4. Regarding applicant's arguments for claim 1, and specifically regarding a "switch", examiner asserts that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). According to the detailed disclosure and applicant's arguments, it appears that applicant intends to use "switch" to mean "a crossbar switch" (applicant's arguments, page 9) and argues that an

arbiter is not a switch. However, claim 1 merely recites a "switch" which means "a device or programming technique for making a selection" (IEEE dictionary, 7th edition, relevant pages attached). Arbitration is defined as "the process of selecting the next bus master" and also as "the process of determining which requesting device will gain access to a resource", both would require a selection is being made. **Based on the above definitions, the connecting facility disclosed by Yamamoto is a switch as it arbitrates communicative access between interface adapters, drive interface adapters, and cache memory**.

Further regarding claim 1, and specifically regarding a "control module", applicant argues that Yamamoto does not teach a control module. To help the applicant better understand examiner's prior rejection, paragraphs 20-23 describe figure 1, which include a terminal interface (administrator, element 43) that is a control module.

Still further regarding claim 1, and specifically regarding "data virtualization", examiner again asserts that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. According to applicant's arguments (page 9), applicant seems to use "data virtualization" to mean "storage virtualization". Although definitions for "storage virtualization" and "virtual storage" are readily available in the IEEE dictionary, "data virtualization" or "virtual data" could not be found. Google defines "virtualization", in the context of computing, as follows: "virtualization involves the process of presenting computing resources in ways that users and applications can easily get value out of them, rather than presenting them in a way dictated by their implementation, geographic location, or physical

packaging. In other words, it provides a logical rather than physical view of data, computing power, storage capacity, and other resources" (definition attached with this action). Throughout Yamamoto's teachings, accessing data on the storage disks is explicitly disclosed as logical volumes that can be converted to physical storage space (for example, see bottom of paragraph 29). **Accordingly, because Yamamoto discloses accessing data in the storage disks as logical volumes, it is data virtualization based on the definition above.**

5. Regarding applicant's arguments for claims 2 and 5, and specifically regarding a "virtual target task", examiner asserts that Yamamoto discloses a TCP/IP interface function (element 70) that receives I/O requests from the host for accessing the storage disks (figure 3 and paragraph 29). The host communicates with the interface like it is a storage unit. Therefore the interface function is a virtual target task.

A similar argument is made regarding a "virtual initiator task". Yamamoto discloses a DIA interface (figure 3; element 86) which communicates with the of drive interface adapters (paragraph 30). The DIA interface communicates with the drive interface adapters through a HIA (host interface adapter) located on the interface adapters (paragraph 31). The process makes the DIA interface (and the NFS interface adapter it is located in) appear to the disk drive as a host. Therefore the function performed by the DIA interface a virtual initiator task.

6. Regarding applicant's arguments for claim 3, and specifically regarding a virtual target and a virtual initiator, examiner asserts that Yamamoto discloses logical volume

which is a virtual target; and the DIA interface recited above (in response to arguments for claims 2 and 5) is a virtual initiator.

7. Regarding applicant's arguments for claims 7 and 8, examiner asserts that the paragraphs 32-34 cited in prior rejection shows DIA interface function being utilized for transmitting data to (write request) and receiving (read request) data from physical storage. DIA interface is associated with the virtual initiator, and is a part of adapters 26-32 that are associated with port processors. Further regarding claim 8, although applicant states that "virtual target translates to two physical targets", applicant fails to state where the translation into two physical targets takes place or the devices involved in this translation into two physical targets. Therefore this limitation is irrelevant to port processors. If applicant intended to state that translation performed by the port processors, Yamamoto teaches that logical/physical address conversion can be performed in adapters 26-32 (paragraph 49).

8. Regarding applicant's arguments for claims 9 and 17, examiner refers applicant to the above argument regarding switch in claim 1 for coupling port processors. Further, examiner refers applicant to figure 1 in which host system is shown as coupled to the storage device through a switch (bus structure, element 16, paragraph 20).

9. Having addressed each of applicant's arguments, examiner maintains the prior rejection. Clarifications are made to more clearly reflect examiner's position.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto (US PUB 2002/0152339 A1).

12. As per claim 1, Yamamoto discloses a storage processing device (system in figure 1), comprising an input/out module (various adapters and connecting facility) including:

Port processors (adapters) to receive and transmit network traffic; (paragraph 22)

And a switch (connecting facility) coupling said port processors; (paragraph 23)

And a control module (terminal interface) coupled to said input/output module, said input/output module and said control module being configured to interactively support data virtualization (logical volume representation of storage, paragraph 29).

13. As per claim 2, Yamamoto discloses the storage processing device of claim 1, wherein said port processors include a port processor (adapter in figure 3) with a frame classification module (logical volume converter), a virtual target task (TCP/IP interface function), and a virtual initiator task (DIA interface function, paragraphs 29,30).

14. As per claim 3, Yamamoto discloses the storage processing device of claim 2, wherein said input/output module and said control module support a virtualization processor (adapter in figure 3) including a virtual target (logical volume), a volume manager mapping block (logical volume access block), and a virtual initiator (DIA interface, paragraphs 29, 30).

15. As per claim 4, Yamamoto discloses volume manager mapping block provides virtual block to physical block mappings (paragraphs 29).

16. As per claim 5, Yamamoto discloses the storage processing device of claim 3, wherein said port processors include a port processor with a frame classification module, a virtual target task, and a virtual initiator task (see rejection for claim 2).

17. As per claim 6, Yamamoto discloses the storage processing device of claim 5, wherein said port processor utilizes said volume mapping block and said virtual target task to translate received frames from a virtual target to a physical target (paragraph 29).

18. As per claim 7, Yamamoto discloses the storage device of claim 6, wherein said port processor utilizes said virtual initiator task to transmit frames to the physical target and receive response frames from the physical target (paragraphs 32-34).

19. As per claim 8, Yamamoto discloses the storage device of claim 8, wherein the virtual target translates to two physical targets (mirror process of RAID) and wherein said port processor utilizes said virtual target task to prepare a command frame for the second physical target and said virtual initiator to transmit said command frame to the second physical target (paragraphs 41, 49, also see rejections for claims 2 and 3).

20. As per claims 9-32, the examiner finds these claims different from claims 1-3 only in statutory category. The references and reasons cited for rejection of claim 1-3 apply in the same manner as applied to claim 1-3. Note that the switch connecting a host and the storage system is shown in figure 1 (bus structure, element 16). A further note is made regarding claims 9 and 17, the limitation of "at least one host and at least two storage devices" is also disclosed by Yamamoto (paragraph 17).

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Sun whose telephone number is (571) 272-2675. The examiner can normally be reached on M-F, 10:30am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS
1/3/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
1/8/06